IN THE CLAIMS:

Claims 1 through 27, 32, 33, and 37 through 47 were previously cancelled. None of the claims have been amended herein. All of the pending claims are presented below for convenience of the Examiner. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

1.-27. (Cancelled)

28. (Previously presented) An integrated circuit comprising:

a semiconductor die;

a plurality of memory cells arranged in at least one array formed on the semiconductor die, each of the plurality of memory cells including at least one container-configured capacitor having a storage node including a roughened outer surface in a substantially vertical dimension with respect to the semiconductor die;

a word line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the word line;

a first digit line formed substantially above the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the first digit line; and

a second digit line formed substantially above the first digit line, wherein the second digit line and the first digit line are separated by an insulated dielectric material.

29. (Previously presented) The integrated circuit of claim 28, further comprising circuitry formed on the semiconductor die and coupled to the memory cells for permitting data to be written to and read from the plurality of memory cells.

30. (Previously presented) The integrated circuit of claim 28, wherein the memory cells are formed with a minimum capable photolithographic feature dimension, and a single one of the memory cells consumes an area of no more than eight times the square of the minimum capable photolithographic feature dimension.

31. (Previously presented) The integrated circuit of claim 28, further comprising a conductive isolation line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the conductive isolation line.

32. (Cancelled)

33. (Cancelled)

34. (Previously presented) The integrated circuit of claim 28, wherein the memory cells are dynamic random access memory cells.

35. (Previously presented) The integrated circuit of claim 28, wherein at least 16,000,000 to 17,000,000 functional and operably addressable memory cells are formed on the semiconductor die.

36. (Previously presented) The integrated circuit of claim 35, wherein all the functional and operably addressable memory cells formed on the semiconductor die have a combined area on the semiconductor die that is no greater than 14 mm^2.

37.-47. (Cancelled)